Remarks

Thorough examination by the Examiner is noted and appreciated.

The claims have been amended to overcome Examiner Section 112 Rejections and further clarify Applicants invention.

No new matter has been added.

For example support is found in the Specification, Figure 1, Figure 7 and in the Specification at:

Beginning at line 10, page 11:

"Shown in Fig. 1 is a semiconductor substrate 10 having formed therein and thereupon an isolation region 12 which defines an active region 10' of the semiconductor substrate 10. As is also shown within the schematic cross-sectional diagram of Fig. 1, **there is a gate electrode 14 formed over the active region 10' of the semiconductor substrate 10 and bridging to the isolation region 12, where, as is understood by a person skilled in the art, the gate electrode 14 covers, and typically defines, a channel region within the active region 10' of the semiconductor substrate 10.** There is also shown within the schematic isometric diagram of Fig. 1 and formed within the active region 10' of the semiconductor substrate 10 a pair of source/drain regions 10a and 10b which is separated by the channel region within the active region 10' of the semiconductor substrate 10 as covered by, and typically defined by, the gate electrode 14. Within the schematic isometric diagram of Fig. 1, the

gate electrode 14 typically and preferably has a linewidth W in a lateral X direction of from about 0.01 to about 1 microns, a thickness T in a vertical Z direction of from about 500 to about 2000 angstroms and a length (not specifically designated) in the longitudinal Y direction of from about 0.2 to about 10 microns".

Beginning at line 10, page 24:

"Shown in Fig. 7 is a schematic cross-sectional diagram of a semiconductor integrated circuit microelectronic fabrication otherwise equivalent to the semiconductor integrated circuit microelectronic fabrication whose schematic cross-sectional diagram is illustrated in Fig. 4, but wherein there is formed within the silicon semiconductor substrate 20 at **a pair of peripheral regions which do not include the corrugated region 20' a pair of isolation regions 32a and 32b which longitudinally define an active region of the semiconductor substrate 20 having the corrugated region 20' of the silicon semiconductor substrate 20 contained therein.**"

Beginning at line 7, page 18:

"Within the preferred embodiment of the present invention, the thermal annealing environment which is employed for forming within the silicon semiconductor substrate 20 the series of thermally grown patterned silicon oxide layers 26a, 26b, 26c and 26d interposed between the series of patterned pad oxide layers 22a, 22b, 22c, 22d and 22e having formed aligned thereupon the series of patterned silicon nitride layers 24a, 24b, 24c, 24d and 24e and extending beneath the series of patterned pad oxide layers 22a, 22b, 22c, 22d and 22e is typically and **preferably provided as an oxidizing thermal annealing environment** at a temperature of from about 700 to about 1100 degrees centigrade for a time period of from about 1 to about 180 minutes, to provide the series of thermally grown patterned silicon oxide layers 26a, 26b, 26c and 26d of thickness from about 100 to about 1000 angstroms and with a curvature generally as illustrated within the schematic cross-sectional diagram of Fig. 3 extending beneath the series of patterned pad oxide layers 22a, 22b, 22c,

22d and 22e."

Beginning at line 13, page 21:

"As is understood by a person skilled in the art, **the series of round bottomed apertures 28a, 28b, 28c and 28d may be formed employing a reactive ion etch (RIE) etch** method as is otherwise conventional in the art of semiconductor integrated circuit microelectronic fabrication, which will typically and preferably employ a chlorine containing etchant gas composition, but with an appropriate and timely addition of a sidewall passivation polymer forming material, such as a bromine containing sidewall passivation polymer forming material, to provide the round bottoms to the series of round bottomed apertures 28a, 28b, 28c and 28d. Typically and preferably, each of series of round bottomed apertures 28a, 28b, 28c and 28d is formed to a depth within the silicon semiconductor substrate 20 of from about 100 to about 1000 angstroms."

Claim Rejections under 35 USC 102

1. Claims 1, 2, 4-6, 9, 9, 11-13 stand rejected under 35 USC 102(b) as being anticipated by Hayashi et al. (US 5,365,078).

Applicants respectfully note that Examiner has previously applied and then withdrawn the application of Hayashi et al., which is now applied again.

Hayashi et al. disclose a device that provides for 1 and 2-dimensional conduction in a **horizontal channel layer formed on** a semiconductor substrate and an **electron supply layer corrugated surface of InAlAs, AlGaAs, or GaAs** (see item 13, Figure 2; col 5, lines 1-5) **formed on the channel layer.** Hayashi et al. disclose the formation of source/drain electrodes and a gate electrode **on the electron supply layer** (see Abstract).

Hayashi et al. do not disclose Applicants disclosed and claimed invention, including a **channel region defined by source and drain regions,** but disclose an electron gas FET where electron charge carriers (electron gas) are conducted through a **horizontal channel layer underlying both the source and drain regions as well as the area underlying the gate electrode** (see

col 1, lines 20-33; lines 47-51; col 2, lines 51-64), rather than a "**gate electrode to cover and define a channel region" as disclosed and claimed by Applicants.**

Thus, Hayashi et al. do not disclose Applicants

"a semiconductor substrate comprising an active region defined by isolation regions"

Hayashi et al. further do not disclose Applicants a " **gate electrode formed over a portion of the active region and at least a portion of the isolation regions to cover and define a channel region** within the active region"

Rather, as stated above, in all embodiments, Hayashi et al. disclose a **corrugated surface** of an **electron supply layer of InAlAs, AlGaAs, or GaAs** (see item 13, Figure 2; col 5, lines 1-5) formed over a horizontal channel layer, which is nowhere disclosed to cover and define a **channel region**. Rather, an electron gas is conducted in a **horizontal channel layer (see e.g., item 12, Figure 2)** extending **under source/drain regions (see items 14 and 15 Figure 2) as well as** the gate electrode. (See also, col 5, lines 36-42, col 6, lines 29-37; col 7, lines

30-35).

Hayashi et al. is clearly insufficient to anticipate Applicants disclosed and claimed invention.

Claim Rejections under 35 USC 103

2. Claims 3, 7, 10, and 14 stand rejected under 35 USC 103(a) as being anticipated by Hayashi et al. (US 5,365,078).

As noted above, Hayashi et al. fail to disclose several elements of Applicants disclosed and claimed invention and therefore fails to produce Applicants disclosed and claimed invention.

As such, Examiners argument "it would have been obvious to one of ordinary skill at the time of the invention to adjust the height of the bumps on the gate electrode to make the transistor with suitable sizes for various applications" and the failure of Applicants to show the critical nature of the height of the "bumps" (peak-to-peak longitudinal periodicity and a peak-to-valley vertical depth) is misplaced.

As pointed out, Hayashi et al. nowhere disclose Applicants

active region defined by isolation regions or Applicants gate electrode structure, or Applicants channel region. Since the requirement of showing a critical nature of a structure is only required to **rebut** a *prima facie* case of overlapping ranges where the structure has been shown in the prior art. For examples see MPEP 2131.03, 2144.05 for the proposition that arguments relating to criticality of dimensions or a necessity of showing unexpected results, both of which are applicable to overlapping ranges, may be **required to rebut a *prima facie* case** where the remaining elements of Applicants structure or method have been shown in the prior art.

Examiner has not shown Applicants structure in the prior art. Nevertheless, Applicants have outlined the benefits of their invention in the Specification, for example see page 30 beginning a line 11:

"With respect to the enhanced performance of the field effect transistor (FET) device fabricated in accord with the present invention, **the enhanced performance is anticipated due to an increased effective channel length and/or gate electrode length** (due to corrugation of the at least one of: (1) the interface of the channel region covered by the gate electrode; and (2) the upper surface of the gate electrode) within the field effect transistor (FET) device fabricated in accord with the present invention. **Such is anticipated to provide an enhanced saturated drain current within the field effect transistor (FET) device in accord with the preferred embodiment of the present invention.**"

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

3. Claims 15-20 stand rejected under 35 USC 103(a) as being unpatentable over Semple et al. (US 6,677,202) in view of Hayashi et al., above.

Since claims 15-20 are dependent claims, Applicants assume Examiner has mistakenly listed claims rejected and has intended to reject one or more of the independent claims.

Applicants reiterate the comments made above with respect to Hayashi et al.

Semple et al. disclose a structure and method for forming a MOS device to reduce channel resistance (see col 1, lines 34-37). The structure and method of Semple et al. disclose forming a corrugated substrate surface (Figure 2A; item 202) and corrugated

overlying gate (Figure 2A, item 207 (see col 1, lines 60-66; col 3, lines 6-14). Semple et al. discloses that the corrugations are **etched with controllable sidewall angles** (oblique portions) (col 3, lines 23-35), and are **shown having planar valley portions and planar peak portions** (see Figures 2A, 4, 3B, and 3D; col 3, line 8, col 4, lines 1-3; claim 1).

Semple et al. further teach that the ratio of the height to the width of the corrugation including the **acute angel of the sidewalls determines the increase in the channel width of the device.** Semple et al. do not disclose or suggest that the top (peak) or bottom (valley) portions of the corrugations be rounded and nowhere discloses a method for forming the same.

Semple et al. nowhere disclose Applicants active region defined by isolation regions or Applicants disclosed and claimed gate structure.

Semple et al. nowhere discloses Applicants corrugated structure for the active region and/or the upper surface of the gate electrode.

On the other hand Hayashi et al. **show** a corrugated surface

having rounded top (peak) or bottom (valley) portions, but **nowhere disclose a method for forming the same.** Rather, Hayashi et al., disclose methods for making a corrugated surface that result in rectangular shaped corrugations (see Figures 6, 10, 11, 12; col 3, lines 52-60; see Figure 7, lines 53-55; col 8, lines 19-42, lines 52-66). Hayashi et al. nowhere discuss or suggest top (peak) or bottom (valley) portions of the corrugations be rounded or disclose a method for forming the same, but rather disclose methods that would result in rectangular "fine line" structures.

Even assuming arguendo, a proper motivation for combining the disparate devices of Hayashi et al. (1 dimensional conduction in a horizontal device of channel layer underlying gate and source and drain regions) with the conventional vertical channel device of Semple et al., such combination does not produce Applicants disclosed and claimed invention.

"Finally, the prior art reference (or references when combined) must teach or suggest **all the claim limitations**. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior

art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

Conclusion

The cited references, alone or in combination, do not produce Applicants disclosed and claimed invention and are therefore insufficient to anticipate or make out a *prima facie* case of obviousness.

The Claims have been amended to clarify Applicants' disclosed and claimed invention. Applicants' respectfully favorable consideration of Applicants claims.

Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in condition for allowance for any reason, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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